Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A logic circuit comprising:
a first inverter having a plurality of linear gate transistors driving a first capacitive load; and
a second inverter having a plurality of cellular gate transistors driving a second capacitive load, said second inverter being connected in series with said second inverter, wherein said second capacitive load is larger than said first capacitive load.

[c2] The logic circuit as in claim 1, wherein said second capacitive load is between about 1.5 to about 3 times larger than said first capacitive load.

[c3] The logic circuit as in claim 1, further comprising a plurality of first inverters and/or a plurality of second inverters.

[c4] The logic circuit as in claim 1, wherein the logic circuit is a circuit selected from the group consisting of a buffer circuit, an oscillator circuit, a digital circuit, and a memory circuit.

[c5] The logic circuit as in claim 1, wherein said plurality of cellular gate transistors comprise a plurality of cells each

having a shape selected from the group consisting of a diamond, a square, a rectangle, a triangle, an octagon, and any combinations thereof.

[c6] A logic circuit comprising:
a first inverter having a plurality of linear gate transistors with a first input capacitance; and
a second inverter being connected in series to said first inverter, said second inverter having a plurality of cellular gate transistors with a second input capacitance, wherein said second input capacitance is at least about one and one-half times larger than said first input capacitance.

[c7] The logic circuit as in claim 6, wherein said second input capacitance is about three times larger than said first input capacitance.

[c8] The logic circuit as in claim 6, wherein said first inverter has a first drain capacitance and said second inverter has a second drain capacitance, wherein said second drain capacitance is at least about one and one-half times larger than said first drain capacitance.

[c9] The logic circuit as in claim 8, wherein said second drain capacitance is about two times larger than said first drain capacitance.

[c10] The logic circuit as in claim 6, wherein said plurality of cellular gate transistors comprise a plurality of cells each having a shape selected from the group consisting of a diamond, a square, a rectangle, a triangle, an octagon, and any combinations thereof.

[c11] The logic circuit as in claim 6, wherein said first inverter drives a first capacitive load and said second inverter drives a second capacitive load, said second capacitive load being larger than said first capacitive load.

[c12] The logic circuit as in claim 11, wherein said second capacitive load is between about 1.5 to about 3 times larger than said first capacitive load.

[c13] A logic circuit comprising:
a first inverter having a plurality of linear gate transistors with a first drain capacitance; and
a second inverter being connected in series to said first inverter, said second inverter having a plurality of cellular gate transistors with a second drain capacitance, wherein said second drain capacitance is at least about one and one-half times larger than said first drain capacitance.

[c14] The logic circuit as in claim 13, wherein said second drain capacitance is about two times larger than said

first drain capacitance.

[c15] The logic circuit as in claim 14, wherein said first inverter has a first input capacitance and said second inverter has a second input capacitance, said second input capacitance being at least about one and one-half times larger than said first input capacitance.

[c16] The logic circuit as in claim 15, wherein said second input capacitance is about three times larger than said first input capacitance.

[c17] The logic circuit as in claim 13, wherein said first inverter drives a first capacitive load and said second inverter drives a second capacitive load, said second capacitive load being larger than said first capacitive load.

[c18] The logic circuit as in claim 17, wherein said second capacitive load is between about 1.5 to about 3 times larger than said first capacitive load.

[c19] The logic circuit as in claim 18, wherein the logic circuit is a circuit selected from the group consisting of a buffer circuit, an oscillator circuit, digital circuits, and memory circuits.